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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,752	12/30/2003	Matthew Mattina	42P17893	9070

59796 7590 07/31/2007

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
07/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/749,752	MATTINA ET AL.
	Examiner	**Art Unit**
	Craig E. Walter	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1 and 3-20 are pending in the Application.

Claims 1, 3 and 18 have been amended.

Claim 2 has been cancelled.

Claims 1 and 3-20 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 12 June 2007 in response to the office action mailed on 12 March 2007 has been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-6, 10,14, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bordaz et al. (US Patent 6,195,728 B1), and in further view of Jennings (US Patent 6,134,631).

As for claims 1, 14 and 18, Bordaz teaches a system (as in claims 1 and 18, and apparatus in claim 14) for maintaining cache coherency in a CMP comprising:

one or more processor cores (Fig. 1, elements 11-14, 31-34, 51-54 and 71-74 depict a plurality of processor cores), wherein the one or more processor cores each include a private cache (each processor contains its own private cache as depicted in Fig. 1 (element 11 is the private cache for processor 1 for example));

a shared cache to be shared by the one or more processor cores (Fig. 1, memory (element 5) is shared among at least two processors));

Note, Bordaz discloses cache memories 5, 15, 45 and 65 which comprise respective remote caches 15, 35, 55 and 77, and the remaining areas of memories 5, 15, 45 and 65 (5', 15', 45' and 65' respectively). In col. 4, line 28 though col. 5, line 7, Bordaz clearly teaches the address space of memories 5', 15', 45' and 65' as being either local or remote (with respect to each memory module 10, 20, 40 or 60). In other words, these memories 5, 15, 45 and 65 are used to store both local and remote data (i.e. shared by another processor from a different memory module). Further evidence that cache memories are "shared" by processors from other modules is seen in the abstract and col. 3, lines 18-47 (invention is aimed at improving cache coherency of a

plurality of modules. Data coherence would not be possible if cache memories where not shared among modules.

and an unbuffered bi-directional ring to connect the one or more processors and the shared cache (Fig. 1, element 16 – the ring is used for communication between each module (elements 10, 20, etc) which each contain the plurality of processors;

Despite these teachings, Bordaz fails to specifically teach these particular elements as being stored on an integrated circuit (i.e. single processor chip). More specifically, Bordaz teaches four discrete modules (Fig. 1, elements 10, 20, 40 and 60) which each comprises multiple processors (each with a unique private cache), and a shared cache.

Jennings teaches a non-volatile memory with embedded programmable controller in which his plurality of modules may all implemented on a single integrated chip (storage system 50 (Fig. 1) may be a multi-chip module, or a single integrated circuit – col. 3, lines 52-58).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Bordaz to implement his discrete modules on a single integrated circuit as taught by Jennings. By doing so, Bordaz could exploit the well-known benefits of single chip integration, which includes lower manufacturing costs, and increased communication speed between the discrete elements implement on the one chip.

It is worthy to note that though Bordaz teaches an "on-module" cache rather than an on-chip cache as recited by Applicant, this would have been obvious over Bordaz as

once all four modules are implemented on a single chip as discussed above in the combined teachings of Bordaz and Jennings. More specifically the shared caches within each module would be stored on that very single chip when Bordaz and Jennings are combined; hence they are "on-chip" cache. It is additionally worthy to note that the shared cache within each module acts as a system memory for storing element held by the shared memory.

As for claim 3, Bordaz teaches the system of claim 1 wherein the shared cache includes one or more cache banks (inherently all cache memory must be arranged in a configuration of at least one bank. Additionally, Bordaz indicates that each shared cache contains a remote access cache (RC – element 15), which is a separate memory bank within the shared cache (element 5)).

As for claim 4, Bordaz teaches wherein the one or more cache banks is responsible for a subset of a physical address space of the system (col. 4, lines 28-46 – the RC (element 15) makes up a portion of the total physical memory of memory element 5).

As for claims 5 and 6, Bordaz teaches the system of claim 1 wherein the one or more processor cores are write-thru, which write data through to the shared cache (col. 7, lines 56-65 – Bordaz discusses a write through cache mechanism which writes to reserved zones in the shared cache (i.e. element 25)).

As for claim 10, Bordaz teaches the system of claim 1 wherein the one or more processor cores accesses data from the shared cache (col. 4, lines 47-53 – each processor accesses data blocks in the shared memories).

As for claims 16 and 19, the shared memory is a shared cache including a plurality of blocks, mad wherein the shared cache is capable of holding each of the plurality of blocks in a cache coherency state (tags are stored and associated with blocks of the cache to indicate which blocks are held exclusively (i.e. to maintain coherency) by a processor - col. 5, lines 21-51).

As for claim 17 and 20, wherein the cache coherency state for each of the plurality of blocks is selected from a group consisting of (1) a not present state, (2) a present and owned by a core of the plurality of cores state, (3) a present, not owned, and custodian is a core of the plurality of core states, and (4) a present, not owned, and no custodian state (the tags include information to indicate if the data is valid and if it is held exclusively by a particular processor – col. 5, lines 21-51).

4. Claims 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Bordaz (US Patent 6,195,728 B1) and Jennings (US Patent 6,134,631) as applied to claim 1 above, and in further view of Fletcher (US Patent 4,445,174).

As for claims 7-9, though Bordaz teaches the system of claim 1, wherein the one or more processor cores include a buffer, he fails to teach the buffer as functioning merge buffer capable of purging stored data to a shared cache.

Fletcher however teaches a multiprocessor system including a shared cache which a processor's private cache (Fig. 1, element 8) continuously stores data (permitting the merging of data (i.e. line by line) into the private memory from the main memory until an eviction is requested) –col. 1, line 62-68, and then moves the lines

directly from a private cache to the shared cache, while circumventing the system's main memory (col. 2, lines 56-64).

As for claim 11, Fletcher further discloses the private cache, which is used to merge data from the memory line by line, as coalescing multiple lines to a same block of the shared cache – col. 3, line 17-25 – copies of the same shared memory block may exist simultaneously in each private cache. In other words, data stored in a processor's private cache can exist as one memory block of the shared memory.

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Bordaz and Jennings to further include Fletcher's multiprocessor system including a shared cache to his own system. By doing so, would realize improved system performance by having a means of automatically detecting lines of information moved to the shared cache, hence eliminating "pingponging" of lines between requesting processors as taught by Fletcher in col. 2, lines 49-65.

5. Claims 12, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Bordaz (US Patent 6,195,728 B1) and Jennings (US Patent 6,134,631) as applied to claims 1 and 14 above, and in further view of Koenen (US PG Publication 2004/0019891 A1).

As for claims 12,13 and 15, though Bordaz teaches connecting his each processor module via a ring configuration as claimed by Applicant in claim 1, he fails to specifically teach the ring configuration as recited by Applicant in claims 12-13 of the pending Application.

Koenen however teaches an apparatus for optimizing performance in a multi-processing system, which includes connecting a plurality of module nodes via a synchronous, unbuffered, bi-directional ring with a fixed deterministic latency as recited by Applicant in claim 12-13. Referring to Fig. 1, a plurality of processing nodes (elements 12, 14 and 16) are connected for bi-directional communication (elements 12J, 14J and 16J) with the interconnect fabric (element 18). Note Koenen describes the fabric as including a ring structure in paragraph 0019, lines 9-12. The ring functions without the aid of a buffering system (i.e. unbuffered), and supports synchronous connections with a minimum static latency around the ring (paragraph 0026, lines 7-12 – the minimum latency is static). Furthermore, paragraph 0023 (and subsequently Table 1), describe preset latencies between each node depending on the number of nodes included in the system. With this table, the overall latency of the entire ring interconnect is known (likewise, fixed), which allows the system to synchronize communication between nodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention, for the combined teachings of Bordaz and Jennings to implement Koenen's apparatus for optimizing performance in a multi-processing system. By doing so, they would benefit by using a superior interconnection fabric (as shown by Koenen in Fig. 1, element 18) for his processing modules, which in turn could help Bordaz's NUMA machine by reducing access latency and increase system performance as taught by Koenen in paragraph 0011, lines 1-15.

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 3-20 have been fully considered, however they are not persuasive.

As for claims 1, 14 and 18, Applicant asserts, "it is clear that only modules 10, 20, 40, and 60 are interconnect by a ring. In direct contrast, applicant's claim 1 includes the element, "a ring to connect the one or more processor cores and the shared cache," (emphasis added). As can be readily seen, processor 1-4 of Bordaz do not connect to cache element 5 in a ring, but rather in a conventional multi-drop interconnect. Therefore, Bordaz only suggests coupling of modules 10, 20, 40, and 60 in a ring, and inclusion of a cache 5 in each module and a private cache in each modules individual processor; however, there is no suggestion or description of a ring to connect the one or more processors and the shared cache," as in applicant's claim 1."

This argument however is not persuasive. Examiner maintains that Bordaz discloses cache memories 5, 15, 45 and 65 which comprise respective remote caches 15, 35, 55 and 77, and the remaining areas of memories 5, 15, 45 and 65 (5', 15', 45' and 65' respectively). In col. 4, line 28 though col. 5, line 7, Bordaz clearly teaches the address space of memories 5', 15', 45' and 65' as being either local or remote (with respect to each memory module 10, 20, 40 or 60). In other words, these memories 5, 15, 45 and 65 are used to store both local and remote data (i.e. shared by another processor from a different memory module). Further evidence that the cache memories are "shared" by processors from other modules is seen in the abstract and col. 3, lines

18-47 (invention is aimed at improving cache coherency of a plurality of modules. Data coherence would not be possible if cache memories where not shared among modules). It is readily apparent from Fig. 1 that the ring (16) connects each module, each containing a shared cache and a plurality of processors.

Applicant further contends "the combination of Bordaz and Jennings is only cited to correct Bordaz' deficiency in regards to the one or more processor cores, the shared cache, and the ring being included in an integrated circuit. However, Jennings does not disclose or suggest coupling a shared cache in a ring with processor cores... neither Bordaz or Jennings discloses coupling of a shared memory and a plurality of cores in a ring, or with an unbuffered bi-directional ring interconnect, on an integrated circuit, as in applicant's claims 14 and 18, respectively."

This argument however is not persuasive. Examiner maintains that Bordaz does in fact teach coupling a shared cache in a ring with processor cores, and that Bordaz in further view of Jennings teach this very configuration on an integrated circuit as per the rejections and arguments presented *supra*.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

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SUPERVISORY PATENT EXAMINER
7/27/07